

an integrated circuit electrically coupled to the first surface of the package substrate, the integrated circuit and the package substrate together forming the semiconductor package;  
a first inductance circuit formed within the semiconductor package; and  
a second inductance circuit formed within the semiconductor package, wherein the first inductance circuit is coupled electrically in parallel to the second inductance circuit, and  
wherein the first and second inductance circuits have substantially symmetrical geometric characteristics.

3. The semiconductor package according to claim 1, further comprising a phase locked loop circuit included within the integrated circuit.

4. The semiconductor package according to claim 3, wherein the phase locked loop circuit comprises a controlled oscillator circuit.

5. The semiconductor package according to claim 4, wherein the controlled oscillator circuit has an output frequency that is selectably operable within a plurality of frequency bands.

6. The semiconductor package according to claim 5, wherein the controlled oscillator circuit comprises an inductor-capacitor tank circuit.

7. The semiconductor package according to claim 6, wherein the inductor-capacitor tank circuit comprises a capacitor electrically coupled to the first and second inductance circuits.

8. The semiconductor package according to claim 7, wherein the first and second inductance circuits are formed entirely within the semiconductor package.

9. The semiconductor package according to claim 1, wherein the integrated circuit comprises a differential amplifier coupled to the parallel combination of the first and second inductance circuits.

10. A semiconductor package, comprising:  
a package substrate having a first surface;  
an integrated circuit electrically coupled to the first surface of the package substrate;  
a first inductance circuit formed within the semiconductor package and formed at least partially between the integrated circuit and the package substrate; and

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a second inductance circuit coupled electrically in parallel with the first inductance circuit, the second inductance circuit formed within the semiconductor package and formed at least partially between the integrated circuit and the package substrate, wherein the first inductance circuit is formed symmetrically with respect to the second inductance circuit.

11. The semiconductor package according to claim 10, wherein the first inductance circuit comprises a first substrate electrical contact on the first surface of the package substrate, wherein the first inductance circuit is formed by first and second conductive features electrically coupled between the integrated circuit and the first substrate electrical contact to form an electrically conductive path.

12. The semiconductor package according to claim 11, wherein the second inductance circuit comprises a second substrate electrical contact on the first surface of the package substrate, wherein the second inductance circuit is formed by third and fourth conductive features electrically coupled between the integrated circuit and the second substrate electrical contact to form an electrically conductive path.

13. The semiconductor package according to claim 12, wherein the package substrate comprises a first set of at least two alternative substrate electrical contacts corresponding

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to the first inductance circuit to provide alternate electrical connection points during package assembly for at least one or both of the first and second conductive features of the first inductance circuit, an inductance value of the first inductance circuit being dependent on the identity of the alternative substrate electrical contact selected in the first set of at least two alternative substrate electrical contacts for coupling electrically to at least one or both of the first and second conductive features.

14. The semiconductor package according to claim 13, wherein the package substrate comprises a second set of at least two alternative substrate electrical contacts corresponding to the second inductance circuit to provide alternate electrical connection points during package assembly for at least one or both of the third and fourth conductive features of the second inductance circuit, an inductance value of the second inductance circuit being dependent on the identity of the alternative substrate electrical contact selected in the second set of at least two alternative substrate electrical contacts for coupling electrically to at least one or both of the third and fourth conductive features.

15. The semiconductor package according to claim 14, wherein the first set of alternative substrate electrical contacts comprises alternative substrate bonding pads disposed at variable distances from the integrated circuit, and wherein the first and second conductive features of the first inductance circuit comprise first and second wire bonds electrically coupled to a selected one of the alternative substrate bonding pads to form an

electrically conductive path having an inductance value at least partially dependent on at least one of the lengths of the first and second wire bonds, the distance between the first and second wire bonds, or both.

16. The semiconductor package according to claim 15, wherein the second set of alternative substrate electrical contacts comprises alternative substrate bonding pads disposed at variable distances from the integrated circuit, and wherein the third and fourth conductive features of the second inductance circuit comprise third and fourth wire bonds electrically coupled to a selected one of the alternative substrate bonding pads to form an electrically conductive path having an inductance value at least partially dependent on at least one of the lengths of the third and fourth wire bonds, the distance between the third and fourth wire bonds, or both.

17. The semiconductor package according to claim 14, wherein the first set of alternative substrate electrical contacts corresponding to the first inductance circuit comprises alternative pairs of first and second substrate bonding pads positioned at variable locations on or within the package substrate, each of the first and second substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a fifth conductive feature, and wherein the first and second conductive features of the first inductance circuit comprise first and second solder

bumps positioned so that they are electrically coupled to a selected respective alternative pair of first and second substrate bonding pads to form an electrically conductive path.

18. The semiconductor package according to claim 17, wherein the second set of alternative substrate electrical contacts corresponding to the second inductance circuit comprises alternative pairs of third and fourth substrate bonding pads positioned at variable locations on or within the package substrate, each of the third and fourth substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a sixth conductive feature, and wherein the third and fourth conductive features of the second inductance circuit comprise third and fourth solder bumps positioned so that they are electrically coupled to a selected respective alternative pair of third and fourth substrate bonding pads to form an electrically conductive path.

19. The semiconductor package according to claim 14, wherein the first set of alternative substrate electrical contacts corresponding to the first inductance circuit comprises alternative pairs of first and second substrate bonding pads positioned at variable locations on or within the package substrate, each of the first and second substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a fifth conductive feature, and wherein the first and second conductive features of the first inductance circuit comprise first and second wire

bonds electrically coupled to a selected respective alternative pair of first and second substrate bonding pads to form an electrically conductive path.

20. The semiconductor package according to claim 19, wherein the second set of alternative substrate electrical contacts corresponding to the second inductance circuit comprises alternative pairs of third and fourth substrate bonding pads positioned at variable locations on or within the package substrate, each of the third and fourth substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a sixth conductive feature, and wherein the third and fourth conductive features of the second inductance circuit comprise third and fourth wire bonds electrically coupled to a selected respective alternative pair of third and fourth substrate bonding pads to form an electrically conductive path.

21. The semiconductor package according to claim 14, wherein the integrated circuit comprises a differential amplifier coupled to the parallel combination of the first and second inductance circuits.

22. A method of assembling a semiconductor package, comprising:  
providing a package substrate having a first surface;  
including within the semiconductor package an integrated circuit electrically coupled to the package substrate;

forming a first inductance circuit within the semiconductor package, the first inductance being formed at least partially between the integrated circuit and the package substrate; and

forming a second inductance circuit within the semiconductor package, the second inductance being formed at least partially between the integrated circuit and the package substrate, the second inductance circuit being coupled electrically in parallel with the first inductance circuit,

wherein the first and second inductance circuits are formed within the semiconductor package so that an interfering magnetic signal induces a common-mode signal in the parallel combination of the first and second inductance circuits.

23. The method according to claim 22, wherein forming the first inductance circuit further comprises:

providing a first substrate electrical contact on the first surface of the package substrate; and

coupling electrically first and second conductive features between the integrated circuit and the first substrate electrical contact to form an electrically conductive path.



24. The method according to claim 23, wherein forming the second inductance circuit further comprises:

providing a second substrate electrical contact on the first surface of the package substrate; and

coupling electrically third and fourth conductive features between the integrated circuit and the first substrate electrical contact to form an electrically conductive path.

25. The method according to claim 24, wherein forming the first inductance circuit further comprises:

including within the package substrate a first set of at least two alternative substrate electrical contacts corresponding to the first inductance circuit to provide alternate electrical connection points during package assembly for at least one or both of the first and second conductive features of the first inductance circuit,

wherein an inductance value of the first inductance circuit depends on the identity of the alternative substrate electrical contact selected in the first set of at least two alternative substrate electrical contacts for coupling electrically to at least one or both of the first and second conductive features.

26. The method according to claim 25, wherein forming the second inductance circuit further comprises:

including within the package substrate a second set of at least two alternative substrate electrical contacts corresponding to the second inductance circuit to provide alternate electrical connection points during package assembly for at least one or both of the third and fourth conductive features of the second inductance circuit,

wherein an inductance value of the second inductance circuit depends on the identity of the alternative substrate electrical contact selected in the second set of at least two alternative substrate electrical contacts for coupling electrically to at least one or both of the third and fourth conductive features.

27. The method according to claim 26, wherein the first set of alternative substrate electrical contacts comprises alternative substrate bonding pads disposed at variable distances from the integrated circuit, and wherein the first and second conductive features of the first inductance circuit comprise first and second wire bonds electrically coupled to a selected one of the alternative substrate bonding pads to form an electrically conductive path having an inductance value at least partially dependent on at least one of the lengths of the first and second wire bonds, the distance between the first and second wire bonds, or both.

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28. The method according to claim 27, wherein the second set of alternative substrate electrical contacts comprises alternative substrate bonding pads disposed at variable distances from the integrated circuit, and wherein the third and fourth conductive features of the second inductance circuit comprise third and fourth wire bonds electrically coupled to a selected one of the alternative substrate bonding pads to form an electrically conductive path having an inductance value at least partially dependent on at least one of the lengths of the third and fourth wire bonds, the distance between the third and fourth wire bonds, or both.

29. The method according to claim 26, wherein the first set of alternative substrate electrical contacts corresponding to the first inductance circuit comprises alternative pairs of first and second substrate bonding pads positioned at variable locations on or within the package substrate, each of the first and second substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a fifth conductive feature, and wherein the first and second conductive features of the first inductance circuit comprise first and second solder bumps positioned so that they are electrically coupled to a selected respective alternative pair of first and second substrate bonding pads to form an electrically conductive path.

30. The method according to claim 29, wherein the second set of alternative substrate electrical contacts corresponding to the second inductance circuit comprises alternative pairs of third and fourth substrate bonding pads positioned at variable locations on or within the package substrate, each of the third and fourth substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a sixth conductive feature, and wherein the third and fourth conductive features of the second inductance circuit comprise third and fourth solder bumps positioned so that they are electrically coupled to a selected respective alternative pair of third and fourth substrate bonding pads to form an electrically conductive path.

31. The method according to claim 26, wherein the first set of alternative substrate electrical contacts corresponding to the first inductance circuit comprises alternative pairs of first and second substrate bonding pads positioned at variable locations on or within the package substrate, each of the first and second substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a fifth conductive feature, and wherein the first and second conductive features of the first inductance circuit comprise first and second wire bonds electrically coupled to a selected respective alternative pair of first and second substrate bonding pads to form an electrically conductive path.

32. The method according to claim 31, wherein the second set of alternative substrate electrical contacts corresponding to the second inductance circuit comprises alternative pairs of third and fourth substrate bonding pads positioned at variable locations on or within the package substrate, each of the third and fourth substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a sixth conductive feature, and wherein the third and fourth conductive features of the second inductance circuit comprise third and fourth wire bonds electrically coupled to a selected respective alternative pair of third and fourth substrate bonding pads to form an electrically conductive path.

33. The method according to claim 26, further comprising providing a phase locked loop circuit within the integrated circuit, the phase locked loop circuit being electrically coupled to the first and second inductance circuits.

34. The method according to claim 33, further comprising including a controlled oscillator circuit within the phase locked loop circuit.

35. The method according to claim 34, wherein the controlled oscillator circuit has an output frequency that is selectably operable within a plurality of frequency bands.